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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/950,026	PHAM, MANH HUNG	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

SECOND DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Brisse et al. (WO 99/05599). As per claims 1 and 17, Brisse et al. discloses detecting a memory error; analyzing said memory error, determining a memory module in which said error occurred and creating a log; and storing said log in said non-volatile memory section of said memory module on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings.

3. As per claims 2 and 18, Brisse et al. discloses wherein said memory error is detected during a diagnostic test on pages 8 and 9, 'In another embodiment of the invention, memory errors may be detected during manufacture...This embodiment may be utilized in manufacturing test images and systems undergoing hot room testing.'

4. As per claims 3 and 19, Brisse et al. discloses wherein said memory error is detected during normal operation on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings. These embodiments are inclusive of detecting errors during normal operation.

5. As per claims 4 and 20, Brisse et al. discloses wherein said log comprises information about the error type on page 4, beginning at 'As discussed in detail below,

the driver 2 periodically polls' thru page 5, ending at 'Although the single bit error register provides a partial address, it should be understood that the full address relates to specific memory location on one of the error correctable memory chips.'

6. As per claims 5 and 21, Brisse et al. discloses wherein said log comprises information about the location of the memory module on pages 6 and 7, 'The interface slot number identifying the slot having the memory chip 6 with the error may be determined by accessing the command register to determining whether the error correctable memory is interleaved and to identify the memory interface slots that are in use.'

7. As per claims 6,15,22,31, Brisse et al. discloses wherein said log comprises information about the date and time when said error occurred on page 8, 'Accordingly, when a second...error is detected during this twenty-eight day time period, all error stored in the storage medium that have occurred within the period and that have not been logged to the Event Log are then be logged with their original time stamps.'

8. As per claims 7 and 23, Brisse et al. discloses wherein said log comprises information about the system identification on page 7, 'As is known in the art, the system registry is a system database maintained by the operating system to store data such as, for example system configuration information, installation information, and information relating to installed hardware and software devices.'

9. As per claims 8 and 24, Brisse et al. discloses wherein said log is stored in a cyclical manner on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings.

10. As per claims 9 and 25, Brisse et al. discloses a central processing unit; a memory system coupled with said central processing unit comprising a plurality of memory module slots for receiving of memory modules, said memory module comprising a random access memory section and a non-volatile memory section; means for detecting an error in said memory system; means for generating a log about said error; and means for storing said log in said non-volatile memory section of a memory module on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings; on page 3, beginning at 'Computer systems...' thru page 4, ending at 'The system further includes...' It is inherent for the chipset to have RAM in association with the CPU.

11. As per claims 10 and 26, Brisse et al. fails to explicitly state wherein said means for detecting an error generate an exception within said central processing unit on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings. The exception is the error detection signal.

12. As per claims 11 and 27, Brisse et al. discloses wherein said non-volatile memory is divided in a plurality of sub sections each sub section storing one log on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings and on page 4, beginning at 'As discussed in detail below, the driver 2 periodically polls' thru page 5, ending at 'Although the single bit error register provides a partial address, it should be understood that the full address relates to specific memory location on one of the error correctable memory chips.'.

13. As per claims 12 and 28, Brisse et al. discloses wherein said sub sections are written in a cyclical manner on page 1, under the Summary of the Invention – page 2, before the Brief Description of the Drawings.

14. As per claims 13 and 29, Brisse et al. discloses wherein said log comprises information about the error type on page 4, beginning at 'As discussed in detail below, the driver 2 periodically polls' thru page 5, ending at 'Although the single bit error register provides a partial address, it should be understood that the full address relates to specific memory location on one of the error correctable memory chips.'

15. As per claims 14 and 30, Brisse et al. discloses wherein said log comprises information about the location of the memory module on pages 6 and 7, 'The interface slot number identifying the slot having the memory chip 6 with the error may be determined by accessing the command register to determining whether the error correctable memory is interleaved and to identify the memory interface slots that are in use.'

16. As per claims 16 and 32, Brisse et al. discloses wherein said log comprises information about the system identification on page 7, 'As is known in the art, the system registry is a system database maintained by the operating system to store data such as, for example system configuration information, installation information, and information relating to installed hardware and software devices.'

Response to Arguments

17. Applicant's arguments filed 10/18/2004 have been fully considered and the previous rejection has been withdrawn due to the affidavit/declaration submitted;

however, a new rejection has been made under Brisse et al. as indicated above in the rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Yolanda Wilson
Examiner
Art Unit 2113

ylw

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
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